REMARKS

Claims 1-74 are currently pending in the application; claims 3, 4, 6, 8-10, 12, 15, 16, 18, 20-22, 24, 26-30, 32-34, 36-54, 56-71 and 73 are withdrawn from consideration. Claims 1, 60, 61 and 72 have been amended. Claim 55 has been cancelled without prejudice. Support for the amendments is found, for example, from Page 29, Paragraph 3 to Page 30, Paragraph 2 of the specification and Figures 6-10 of the drawings. No new matter has been introduced by the amendment.

Initially, Applicants would like to thank the Examiner for the indication that claims 13, 14, 17, 19, 23, 25, 31, 35 and 74 are allowable. The Examiner has objected to claims 11 and 68 as being dependent upon a rejected base claim, but indicated that the claims would be allowable if rewritten in independent form including all of the limitations of any intervening claims.

Applicant respectfully requests the Examiner to enter the amendments made to the claims and reconsider the present application in light of the amendments.

In the previous Final Rejection, the Examiner has rejected claims 1, 55 and 72 under 35 U.S.C. § 102(e) as allegedly anticipated by U.S. Patent No. 6,383,916 issued to Lin (hereinafter "Lin"). The Examiner has rejected claims 2 and 61 under 35 U.S.C. § 103(a) as being unpatentable over Lin in view of U.S. Patent No. 6,137,164 issued to Yew et al., (hereinafter "Yew"). The Examiner has rejected claim 5 under 35 U.S.C. § 103(a) as unpatentable over Yew in view of U.S. Patent No. 6,630,628 issued to Devnani et al., (hereinafter "Devnani"). The Examiner has further rejected claims 7 and 60 under 35 U.S.C. § 103(a) as unpatentable over Lin in view of U.S. Patent No. 6,184,477 issued to Tanahashi ("Tanahashi"). Applicants respectfully submit that the above rejections are overcome in view of the amendments made to the claims and the remarks made herein.

Independent claim 1, as currently amended, recites a semiconductor unit having two device terminals for every one input/output signal. The semiconductor unit includes a laminated substrate and a semiconductor chip. The substrate includes at least two wiring layers, which include a signal wiring layer and a power-supply or ground wiring layer. The substrate has a main surface. The semiconductor chip has an input/output pad and is mounted on the main surface of the laminated substrate through the input/output pad. Significantly, the two device terminals are mounted on the laminated substrate and connected to both ends of a signal wire in the signal wiring layer, and the signal wire is connected to the input/output pad of the semiconductor chip through a via hole formed within the laminated substrate.

Thus, the invention recited by claim 1 contemplates a novel semiconductor configuration wherein two terminals for input/output signals are connected to each other through a signal wire in the wiring layer in a laminated substrate and the wire is further connected to the input/output pad through a via hole also formed in the laminated substrate, as illustrated in Fig. 6 of the application.

Lin discloses a method for forming a top metallization system for high performance integrated circuits, and a semiconductor structure formed by the method. Specifically, the Lin semiconductor structure is used to "elevate or fan-out the fine-line interconnects and to remove these interconnects from the micro and sub-micro level to a metal interconnect level that has considerable larger dimensions and is therefore with smaller resistance and capacitance and is easier and more cost effective to manufacture" (see Col. 6, Lines 49-54). Lin discloses a semiconductor structure, as shown from Figs. 1-8 thereof, including a plurality of signal pads (6) (contact points in micro and sub-micro level) connected to a plurality of contact pads (10) (metal level pads) through a via (7).

As illustrated in Figs. 9-11, Lin further extends the above design concept to BGA (Ball Grid Array) substrates by connecting the relatively crowded and smaller contact balls at one side of the substrates to the relatively loosely distributed and bigger contact balls at the other side of the substrates through wires disposed in the substrates, thereby "the BGA pads can be arranged in a different and arbitrary sequence that is required for further circuit design or packaging" (see Col. 8, Lines 14-16 of Lin). As shown in Figs. 9-11, the BGA substrate (106 in Figure 9; and 130 in Figures 10 and 11) has a plurality of balls (101-105), which are disposed on the upper side of the substrate and are relatively close to each other. The closely located balls (101-105) are connected to another group of balls (111-115 in Fig. 9; 121-125 in Fig. 10; and 138-142 in Fig. 11), which are relatively larger and distributed loosely on lower side of the substrate, through a group of wires (131, 132, 134, 136).

However, Lin is distinguished from the present invention for at least the following reasons.

First, the via (7) connecting the signal pad (6) and the contact pad (10) is not formed in the BGA substrate (106, 130), in which the wires (131, 132, 134, 136) are formed to connect the balls (101-105) to the balls (111-115, 121-125, and 138-142). In contrast, claim 1 recites that the via hole is formed in the laminated substrate having a wiring layer providing a signal wire connecting the terminal devices. In other words, the via and the wire of the present invention are formed in the same laminated substrate.

Furthermore, Lin does not teach that the wires (131, 132, 134, 136) connecting the contact balls disposed at the opposite sides of the BGA substrate (106, 130) are further connected to the via formed in the same substrate. In contrast, claim 1 recites that the signal wire is connected to the input/output pad of the semiconductor chip through a via hole, in order to connect the device terminals to the input/output pad.

Similarly, independent claims 60 and 61 recite that the two device terminals are connected to each other through a via hole and the via hole is connected to the input/output pad of the semiconductor chip through a wire, both the via hole and the wire formed in the same laminated substrate. In this regard, Lin also fails to disclose that the via hole and the wire are formed in the same laminated substrate, and that the via hole and the wire are connected to each other so as to connect the device terminals to the input/output pad.

Independent claim 72 is directed to a semiconductor unit comprising a semiconductor chip having an input/output pad and a package having a main surface and a back surface. The package comprises at least two ball terminal adhesive areas for every single input/output signal on the main and back surfaces of the package. A ball terminal is adhered to only one ball terminal adhesive area on one surface of the package. The chip pads formed by the two ball terminal adhesive areas make it possible for ease of suitable wiring layouts. Significantly, the two ball terminal adhesive areas are connected to each other through a via hole, and the via hole is connected to the input/output pad of the semiconductor chip through a wire, both the via hole and the wire formed in the same package. In this regard, Lin fails to disclose that the via hole and the wire are formed in the same package, and that the via hole and the wire are connected to each other so as to connect the terminals adhesive areas of the package to the input/output pad of the semiconductor chip.

Since Lin fails to disclose each and every element of claims 1 and 72, as amended, the rejection of claims 1 and 72 under 35 U.S.C. §102(e) based on Lin is overcome.

Tanahashi discloses a multi-layer circuit substrate having orthogonal grid ground and power planes. Tanahashi is relied on to allegedly teach a substrate implementing terminals connections through via holes, recited by claim 60. However, Tanahashi fails to overcome the underlying deficiencies identified in Lin relative to claim 60. Therefore, Lin and Tanahashi, taken

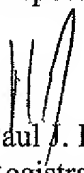
alone or in combination, fail to disclose or suggest the combination of features of claim 60. Accordingly, the rejection of claim 60 under 35 U.S.C. § 103(a) over Lin in view of Tanahashi is overcome.

Yew discloses an assembly for stacking IC devices. Yew is relied on to allegedly teach a substrate having two semiconductor chips mounted on the main surface and back surface respectively, recited by claim 61. However, Yew fails to overcome the underlying deficiencies identified in Lin relative to claim 61. Therefore, Lin and Yew, taken alone or in any proper combination, fail to disclose or suggest the combination of features, as recited in claim 61. Accordingly, the rejection of claim 61 under 35 U.S.C. § 103(a) over Lin in view of Yew is overcome.

Applicants further submit that the rejection to the claims depending from claims 1, 60, 61 and 72 is overcome for at least the reasons stated above.

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application are believed to be in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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